IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently Amended) A method for disposing a material on a semiconductor device structure, comprising:

providing a semiconductor device structure including a surface and at least one recess formed in ~~said~~ the surface;

disposing ~~said~~ the material on at least a portion of ~~said~~ the surface so as to substantially fill ~~said~~ the at least one recess, ~~said~~ the material covering ~~said~~ the surface having a thickness less than a depth of ~~said~~ the at least one recess without subsequently removing ~~said~~ the material from ~~said~~ the surface, the material forming a layer of non-uniform thickness with an upper surface ~~of said material being~~ that is substantially planar.

2. (Currently Amended) The method of claim 1, wherein ~~said~~ disposing comprises disposing ~~said~~ the material so as to substantially fill ~~said~~ the at least one recess without substantially covering ~~said~~ the surface.

3. (Currently Amended) The method of claim 1, wherein ~~said~~ disposing comprises:

applying ~~said~~ the material to ~~said~~ the surface of ~~said~~ the semiconductor device structure;

spinning ~~said~~ the semiconductor device structure;

decreasing a rate of ~~said~~ the spinning while permitting ~~said~~ the material to at least partially cure; and

gradually increasing ~~said~~ the rate of ~~said~~ spinning.

4. (Currently Amended) The method of claim 3, further comprising exposing ~~said~~ the material to a soft baking temperature following ~~said~~ the gradually increasing.

5. (Currently Amended) The method of claim 3, wherein ~~said~~ spinning is effected at a rate of about 1,000 rpm.

6. (Currently Amended) The method of claim 3, wherein ~~said~~ decreasing ~~said~~ the rate comprises decreasing ~~said~~ the rate of ~~said~~ the spinning to about 100 rpm.

7. (Currently Amended) The method of claim 3, wherein ~~said~~ gradually increasing ~~said~~ the rate comprises gradually increasing ~~said~~ the rate of ~~said~~ spinning to at least about 1,000 rpm.

8. (Currently Amended) The method of claim 1, wherein, upon exposing ~~said~~ the material disposed over an entirety of ~~said~~ the semiconductor device structure to an etchant, ~~said~~ the material covering ~~said~~ the surface is substantially removed therefrom, while ~~said~~ the material located in ~~said~~ the at least one recess substantially fills ~~said~~ the at least one recess.

9. (Currently Amended) The method of claim 1, wherein ~~said~~ providing ~~said~~ the semiconductor device structure comprises providing a stacked capacitor structure with ~~said~~ the at least one recess comprising at least one container formed in an insulator layer of ~~said~~ the stacked capacitor structure, ~~said~~ the surface and ~~said~~ the at least one container being lined with a conductive material.

10. (Currently Amended) The method of claim 9, wherein ~~said~~ providing ~~said~~ the semiconductor device structure comprises providing ~~said~~ the stacked capacitor structure with ~~said~~ the surface and ~~said~~ the at least one container being lined with doped hemispherical grain polysilicon.

11. (Currently Amended) The method of claim 9, wherein ~~said~~ disposing ~~said~~ the material comprises disposing a mask material over ~~said~~ the semiconductor device structure.

12. (Currently Amended) The method of claim 1, wherein ~~said~~ providing ~~said~~ the semiconductor device structure comprises providing a shallow trench isolation structure with ~~said~~ the at least one recess comprising at least one trench formed in a surface of ~~said~~ the shallow trench isolation structure.

13. (Currently Amended) The method of claim 12, wherein ~~said~~ disposing ~~said~~ the material comprises disposing a mask material over ~~said~~ the shallow trench isolation structure.

14. (Currently Amended) The method of claim 12, wherein ~~said~~ providing ~~said~~ the shallow trench isolation structure comprises providing ~~said~~ the shallow trench isolation structure with an insulator layer substantially filling ~~said~~ the at least one trench and covering ~~said~~ the surface.

15. (Currently Amended) The method of claim 14, wherein ~~said~~ disposing ~~said~~ the material comprises disposing a stress buffer over ~~said~~ the insulator layer, ~~said~~ the stress buffer having a substantially planar surface without removing material thereof following ~~said~~ disposing.

16. (Currently Amended) The method of claim 1, wherein ~~said~~ providing comprises providing a semiconductor device structure having a surface with at least one dual damascene trench recessed therein and a layer of conductive material with a nonplanar surface disposed in ~~said~~ the at least one dual damascene trench and at least partially covering ~~said~~ the surface.

17. (Currently Amended) The method of claim 16, wherein ~~said~~ disposing ~~said~~ the material comprises disposing a stress buffer over ~~said~~ the layer of conductive material, ~~said~~ the stress buffer having a substantially planar surface without removing material thereof following ~~said~~ disposing.

18. (Withdrawn—Currently Amended) A method for masking a stacked capacitor structure, comprising:

providing a semiconductor device structure with a stacked capacitor structure including:

an insulator layer;

at least one container formed in ~~said~~ the insulator layer; and

a layer of conductive material covering a surface of ~~said~~ the insulator layer and lining ~~said~~ the at least one container;

applying a layer of masked material to ~~said~~ the semiconductor device structure; and

spreading ~~said~~ the mask material across ~~said~~ the semiconductor device structure so as to substantially fill ~~said~~ the at least one container and cover ~~said~~ the layer of conductive material over ~~said~~ the surface with a thickness of about less than half a depth of ~~said~~ the at least one container.

19. (Withdrawn—Currently Amended) The method of claim 18, wherein ~~said~~ providing ~~said~~ the semiconductor device structure comprises providing a semiconductor device structure with ~~said~~ the layer of conductive material of ~~said~~ the stacked capacitor structure comprising hemispherical grain polysilicon.

20. (Withdrawn—Currently Amended) The method of claim 18, wherein ~~said~~ spreading comprises spinning ~~said~~ the mask material across ~~said~~ the semiconductor device structure.

21. (Withdrawn—Currently Amended) The method of claim 20, wherein ~~said~~ spinning comprises:

rotating ~~said~~ the semiconductor device structure at a first speed;

decreasing a rate of ~~said~~ rotating to a second speed; and

gradually increasing ~~said~~ the rate of ~~said~~ rotating to a third speed.

22. (Withdrawn—Currently Amended) The method of claim 21, wherein ~~said~~ decreasing ~~said~~ the rate follows ~~said~~ rotating.

23. (Withdrawn—Currently Amended) The method of claim 22, wherein ~~said~~ gradually increasing ~~said~~ the rate follows ~~said~~ the decreasing ~~said~~ the rate.

24. (Withdrawn—Currently Amended) The method of claim 18, wherein ~~said~~ spreading comprises substantially filling ~~said~~ the at least one container with ~~said~~ the mask material while leaving ~~said~~ the layer of conductive material covering ~~said~~ the surface substantially uncovered by ~~said~~ the mask material.

25. (Withdrawn—Currently Amended) The method of claim 18, further comprising removing ~~said~~ the layer of conductive material covering ~~said~~ the surface.

26. (Withdrawn—Currently Amended) The method of claim 25, wherein ~~said~~ removing comprises etching ~~said~~ the layer of conductive material.

27. (Withdrawn—Currently Amended) The method of claim 26, wherein ~~said~~ etching comprises wet etching ~~said~~ the layer of conductive material.

28. (Withdrawn—Currently Amended) The method of claim 26, wherein ~~said~~ etching comprises dry etching ~~said~~ the layer of conductive material.

29. (Withdrawn—Currently Amended) The method of claim 25, wherein during ~~said~~ removing ~~said~~ the at least one container remains substantially filled with ~~said~~ the mask material.

30. (Withdrawn—Currently Amended) The method of claim 25, further comprising removing ~~said~~ the mask material from ~~said~~ the at least one container.

31. (Withdrawn—Currently Amended) A method for forming a shallow trench isolation structure, comprising:

providing a semiconductor substrate with a surface and at least one shallow trench recessed in ~~said~~ the surface;

applying mask material to ~~said~~ the semiconductor substrate;

spreading ~~said~~ the mask material across ~~said~~ the semiconductor substrate so as to substantially fill ~~said~~ the at least one shallow trench, ~~said~~ the mask material covering ~~said~~ the surface as a result of ~~said~~ the spreading having a thickness of less than about half a depth of ~~said~~ the at least one shallow trench; and

exposing at least ~~said~~ the mask material to a dopant so as to conductively dope semiconductor material beneath ~~said~~ the surface without substantially doping semiconductor material located beneath ~~said~~ the at least one shallow trench.

32. (Withdrawn—Currently Amended) The method of claim 31, wherein ~~said~~ spreading comprises spinning ~~said~~ the mask material across ~~said~~ the semiconductor substrate.

33. (Withdrawn—Currently Amended) The method of claim 32, wherein ~~said~~ spinning comprises:

rotating ~~said~~ the semiconductor substrate at a first speed;

decreasing a rate of ~~said~~ rotating to a second speed; and

gradually increasing ~~said~~ the rate of ~~said~~ rotating to a third speed.

34. (Withdrawn—Currently Amended) The method of claim 33, wherein ~~said~~ decreasing ~~said~~ the rate follows ~~said~~ rotating.

35. (Withdrawn—Currently Amended) The method of claim 34, wherein ~~said~~ gradually increasing ~~said~~ the rate follows ~~said~~ decreasing ~~said~~ the rate.

36. (Withdrawn—Currently Amended) The method of claim 31, wherein ~~said~~ spreading comprises substantially filling ~~said~~ the at least one shallow trench with ~~said~~ the mask material while leaving ~~said~~ the surface substantially uncovered by ~~said~~ the mask material.

37. (Withdrawn—Currently Amended) The method of claim 31, wherein ~~said~~ exposing includes implanting conductivity dopant into regions of ~~said~~ the semiconductor substrate continuous with ~~said~~ the surface without implanting conductivity dopant into regions of ~~said~~ the semiconductor substrate continuous with a bottom of ~~said~~ the at least one shallow trench.

38. (Withdrawn—Currently Amended) The method of claim 31, further comprising removing ~~said~~ the mask material from ~~said~~ the semiconductor substrate.

39. (Withdrawn—Currently Amended) A method for fabricating a semiconductor device structure, comprising:

providing a semiconductor device structure with a surface, at least one recess formed in ~~said~~ the surface, and a material layer at least partially covering ~~said~~ the surface and substantially filling ~~said~~ the at least one recess, ~~said~~ the material layer having a nonplanar surface;

applying a stress buffer material to ~~said~~ the material layer; and

spreading ~~said~~ the stress buffer material over ~~said~~ the material layer so as to impart ~~said~~ the stress buffer material with a substantially planar surface without subsequently planarizing ~~said~~ the stress buffer material.

40. (Withdrawn—Currently Amended) The method of claim 39, wherein ~~said~~ providing comprises providing ~~said~~ the semiconductor device structure with ~~said~~ the nonplanar surface of ~~said~~ the material layer including at least one peak located substantially over ~~said~~ the surface and at least one valley located substantially over ~~said~~ the at least one recess.

41. (Withdrawn—Currently Amended) The method of claim 39, wherein ~~said~~ spreading comprises spinning ~~said~~ the stress buffer material across ~~said~~ the semiconductor device structure.

42. (Withdrawn—Currently Amended) The method of claim 41, wherein ~~said~~ the spinning comprises:
rotating ~~said~~ the semiconductor device structure at a first speed;
decreasing a rate of ~~said~~ rotating to a second speed; and
gradually increasing ~~said~~ the rate of ~~said~~ rotating to a third speed.

43. (Withdrawn—Currently Amended) The method of claim 42, wherein ~~said~~ decreasing ~~said~~ the rate follows ~~said~~ rotating.

44. (Withdrawn—Currently Amended) The method of claim 43, wherein ~~said~~ gradually increasing ~~said~~ the rate follows ~~said~~ decreasing ~~said~~ the rate.

45. (Withdrawn—Currently Amended) The method of claim 40, wherein ~~said~~ spreading comprises at least partially filling ~~said~~ the at least one valley with ~~said~~ the stress buffer material while leaving ~~said~~ the at least one peak substantially uncovered by ~~said~~ the stress buffer material.

46. (Withdrawn—Currently Amended) The method of claim 45, further comprising planarizing at least ~~said~~ the material layer.

47. (Withdrawn—Currently Amended) The method of claim 46, wherein ~~said~~ planarizing comprises etching at least one region of ~~said~~ the material layer exposed through ~~said~~ the stress buffer material with selectivity over ~~said~~ the stress buffer material.

48. (Withdrawn—Currently Amended) The method of claim 47, wherein ~~said~~ etching is effected until a surface of ~~said~~ the at least one region is in substantially the same plane as ~~said~~ the substantially planar surface of ~~said~~ the stress buffer material.

49. (Withdrawn—Currently Amended) The method of claim 48, wherein ~~said~~ planarizing further comprises abrasively planarizing ~~said~~ the stress buffer material and ~~said~~ the at least one region to expose ~~said~~ the surface adjacent ~~said~~ the at least one recess, ~~said~~ the surface and a surface of material in ~~said~~ the at least one recess being located in substantially the same plane following ~~said~~ the planarizing.

50. (Withdrawn—Currently Amended) The method of claim 48, wherein ~~said~~ planarizing further comprises concurrently etching ~~said~~ the material layer and ~~said~~ the stress buffer material at substantially the same rate so as to expose ~~said~~ the surface adjacent ~~said~~ the at least one recess with ~~said~~ the surface and a surface of material in ~~said~~ the at least one recess being located in substantially the same plane following ~~said~~ the planarizing.

51. (Withdrawn—Currently Amended) The method of claim 47, wherein ~~said~~ etching is effected until ~~said~~ the surface of ~~said~~ the semiconductor device structure is exposed through ~~said~~ the material layer.

52. (Withdrawn—Currently Amended) The method of claim 51, wherein ~~said~~ etching is effected until a surface of material in ~~said~~ the at least one recess is in substantially the same plane as ~~said~~ the surface.

53. (Withdrawn—Currently Amended) The method of claim 51, further comprising removing ~~said~~ the stress buffer material from ~~said~~ the semiconductor device structure.

54. (Withdrawn—Currently Amended) The method of claim 40, wherein ~~said~~ spreading comprises forming a substantially planar surface over ~~said~~ the semiconductor device structure.

55. (Withdrawn—Currently Amended) The method of claim 54, further comprising planarizing at least ~~said~~ the material layer.

56. (Withdrawn—Currently Amended) The method of claim 55, wherein ~~said~~ planarizing comprises substantially concurrently abrasively planarizing ~~said~~ the stress buffer material and ~~said~~ the material layer to expose ~~said~~ the surface adjacent ~~said~~ the at least one recess, ~~said~~ the surface and a surface of material in ~~said~~ the at least one recess being located in substantially the same plane following ~~said~~ planarizing.

57. (Withdrawn—Currently Amended) The method of claim 55, wherein ~~said~~ planarizing comprises substantially concurrently etching ~~said~~ the material layer and ~~said~~ the stress buffer material at substantially the same rate so as to expose ~~said~~ the surface adjacent ~~said~~ the at least one recess with ~~said~~ the surface and a surface of material in ~~said~~ the at least one recess being located in substantially the same plane following ~~said~~ planarizing.

58. (Withdrawn—Currently Amended) The method of claim 39, wherein ~~said~~ providing ~~said~~ the semiconductor device structure comprises providing a shallow trench isolation structure with ~~said~~ the at least one recess comprising at least one trench and ~~said~~ the material layer comprising electrical insulator material.

59. (Withdrawn—Currently Amended) The method of claim 39, wherein ~~said~~ providing comprises providing a semiconductor device structure with at least one recess comprising a dual damascene trench and ~~said~~ the material layer comprising conductive material.

60. (Withdrawn—Currently Amended) A method for preparing a surface of a semiconductor device structure for planarization, comprising:

providing a semiconductor device structure including at least one recess formed in a surface thereof and a first material layer substantially filling ~~said~~ the at least one recess and covering ~~said~~ the surface, ~~said~~ the first material layer having a nonplanar surface;

applying a second material to ~~said~~ the first material layer; and

spreading ~~said~~ the second material over ~~said~~ the first material layer so as to form a second material layer having a substantially planar surface without requiring subsequent planarization of ~~said~~ the second material.

61. (Withdrawn—Currently Amended) The method of claim 60, wherein ~~said~~ applying ~~said~~ the second material comprises applying a layer of stress buffer material to ~~said~~ the first material layer.

62. (Withdrawn—Currently Amended) The method of claim 60, wherein ~~said~~ spreading comprises:

spinning ~~said~~ the semiconductor device structure at a first speed;

gradually decreasing a rate of ~~said~~ spinning to a second speed; and

gradually increasing a rate of ~~said~~ spinning to a third speed.

63. (Withdrawn—Currently Amended) The method of claim 62, wherein spinning ~~said~~ the semiconductor device structure at ~~said~~ the second speed comprises permitting ~~said~~ the second material within ~~said~~ the at least one recess to at least partially set.

64. (Withdrawn—Currently Amended) The method of claim 62, wherein spinning ~~said~~ the semiconductor device structure at ~~said~~ the third speed comprises forming ~~said~~ the second material over ~~said~~ the surface to a desired thickness.

65. (Withdrawn—Currently Amended) The method of claim 60, wherein ~~said~~ providing comprises providing a shallow trench isolation structure with ~~said~~ the at least one recess comprising at least one trench formed in a surface of ~~said~~ the shallow trench isolation structure.

66. (Withdrawn—Currently Amended) The method of claim 65, wherein ~~said~~ providing further comprises providing ~~said~~ the shallow trench isolation structure with ~~said~~ the first material layer comprising an electrical insulator material.

67. (Withdrawn—Currently Amended) The method of claim 60, wherein ~~said~~ providing comprises providing a semiconductor device structure with ~~said~~ the at least one recess comprising at least one dual damascene trench formed therein.

68. (Withdrawn—Currently Amended) The method of claim 67, wherein ~~said~~ providing further comprises providing a semiconductor device structure with ~~said~~ the first material layer comprising conductive material.

69. (Withdrawn—Currently Amended) The method of claim 61, wherein ~~said~~ spreading comprises at least partially filling at least one valley of ~~said~~ the first material layer with ~~said~~ the stress buffer material while leaving at least one peak of ~~said~~ the first material layer substantially uncovered by ~~said~~ the stress buffer material.

70. (Withdrawn—Currently Amended) The method of claim 69, further comprising planarizing at least ~~said~~ the first material layer.

71. (Withdrawn—Currently Amended) The method of claim 70, wherein ~~said~~ planarizing comprises etching at least one region of ~~said~~ the first material layer exposed through ~~said~~ the stress buffer material with selectivity over ~~said~~ the stress buffer material.

72. (Withdrawn—Currently Amended) The method of claim 71, wherein ~~said~~ etching is effected until a surface of ~~said~~ the at least one region is in substantially the same plane as a surface of ~~said~~ the stress buffer material.

73. (Withdrawn—Currently Amended) The method of claim 72, wherein ~~said~~ planarizing further comprises abrasively planarizing ~~said~~ the stress buffer material and ~~said~~ the at least one region to expose ~~said~~ the surface of ~~said~~ the semiconductor device structure adjacent ~~said~~ the at least one recess, ~~said~~ the surface of ~~said~~ the semiconductor device structure and a surface of ~~said~~ the first material layer in ~~said~~ the at least one recess being located in substantially the same plane following ~~said~~ the planarizing.

74. (Withdrawn—Currently Amended) The method of claim 72, wherein ~~said~~ planarizing further comprises concurrently etching ~~said~~ the first material layer and ~~said~~ the stress buffer material at substantially the same rate so as to expose ~~said~~ the surface of ~~said~~ the semiconductor device structure adjacent ~~said~~ the at least one recess with ~~said~~ the surface of ~~said~~ the semiconductor device structure and a surface of ~~said~~ the first material layer in ~~said~~ the at least one recess being located in substantially the same plane following ~~said~~ planarizing.

75. (Withdrawn—Currently Amended) The method of claim 71, wherein ~~said~~ etching is effected until ~~said~~ the surface of ~~said~~ the semiconductor device structure is exposed through ~~said~~ the first material layer.

76. (Withdrawn—Currently Amended) The method of claim 75, wherein ~~said~~ etching is effected until a surface of ~~said~~ the first material layer in ~~said~~ the at least one recess is in substantially the same plane as ~~said~~ the surface of ~~said~~ the semiconductor device structure.

77. (Withdrawn—Currently Amended) The method of claim 75, further comprising removing ~~said~~ the stress buffer material from ~~said~~ the semiconductor device structure.

78. (Withdrawn—Currently Amended) The method of claim 61, wherein ~~said~~ spreading comprises forming a substantially planar surface over ~~said~~ the semiconductor device structure.

79. (Withdrawn—Currently Amended) The method of claim 78, further comprising planarizing at least ~~said~~ the first material layer.

80. (Withdrawn—Currently Amended) The method of claim 79, wherein ~~said~~ planarizing comprises substantially concurrently abrasively planarizing ~~said~~ the stress buffer material and ~~said~~ the first material layer to expose ~~said~~ the surface of ~~said~~ the semiconductor device structure adjacent ~~said~~ the at least one recess, ~~said~~ the surface of ~~said~~ the semiconductor device structure and a surface of ~~said~~ the first material layer in ~~said~~ the at least one recess being located in substantially the same plane following ~~said~~ planarizing.

81. (Withdrawn—Currently Amended) The method of claim 79, wherein ~~said~~ planarizing comprises substantially concurrently etching ~~said~~ the first material layer and ~~said~~ the stress buffer material at substantially the same rate so as to expose ~~said~~ the surface of ~~said~~ the semiconductor device structure adjacent ~~said~~ the at least one recess with ~~said~~ the surface of ~~said~~ the semiconductor device structure and a surface of ~~said~~ the first material layer in ~~said~~ the at least one recess being located in substantially the same plane following ~~said~~ planarizing.

82. (Withdrawn—Currently Amended) A spin coating method, comprising:
applying a material to a substrate;
spinning ~~said~~ the substrate and ~~said~~ the material at a first speed;
decreasing a rate of ~~said~~ the spinning to a second speed; and
gradually increasing a rate of ~~said~~ the spinning to a third speed.

83. (Withdrawn—Currently Amended) The method of claim 82, wherein ~~said~~ spinning ~~said~~ the substrate and ~~said~~ the material at ~~said~~ the first speed comprises substantially filling recesses formed in ~~said~~ the substrate with ~~said~~ the material.

84. (Withdrawn—Currently Amended) The method of claim 82, wherein ~~said~~ decreasing ~~said~~ the rate and spinning ~~said~~ the substrate and ~~said~~ the material at ~~said~~ the second speed comprise permitting ~~said~~ the material located within recesses formed in ~~said~~ the substrate to set.

85. (Withdrawn—Currently Amended) The method of claim 82, wherein spinning ~~said~~ the substrate and ~~said~~ the material at ~~said~~ the third speed comprises forming ~~said~~ the material over a surface of ~~said~~ the substrate to a desired thickness.

86. (Withdrawn—Currently Amended) The method of claim 82, wherein ~~said~~ decreasing ~~said~~ the rate follows ~~said~~ spinning.

87. (Withdrawn—Currently Amended) The method of claim 84, wherein ~~said~~ gradually increasing ~~said~~ the rate follows ~~said~~ decreasing ~~said~~ the rate.

88-101. (Canceled)